

App Note 361: DS21354/DS21554 vs. DS2154 Single Chip Transceivers

This application note provides a list of the differences between Dallas Semiconductor/Maxim Communications Products DS21354/DS21554 and DS2154 single chip transceivers (SCTs). The additional features contained in the DS21354/DS21554 are highlighted along with the additional registers required for support of the new features, HDLC controller, interleaved bus operation (IBO), and JTAG.

1. Introduction

This application note highlights the differences between the DS21354/DS21554 and the DS2154. The DS21354/DS21554 is a superset of the DS2154 maintaining a consistent pin out and register set. All of the original features of the DS2154 have been retained and software created for the DS2154 is transferable to the DS21354/DS21554 with minimal effort. The DS21354 and DS21554 are functionally equivalent with the only difference being the required supply voltage — the DS21354 operates at 3.3V and the DS21554 operates at 5V.

2. Additional Functionality

New Features	Data Sheet Section
HDLC controller	15
JTAG	17
8 Mbps interleaved PCM bus operation	18
3.3V operation with 5V tolerant I/O (for DS21354)	17

3. Changes in Register Definitions

When implementing the new features of the DS21354/DS21554, a priority was placed on preserving the DS2154's register map to facilitate code migration from existing DS2154 designs. This section highlights register additions and differences found in the DS21354/DS21554.

3.1 New Feature Register Usage

Highlights new registers related to new features. Each item can be found in the data sheet under the listed sections.

3.1.1 Common Control Register

Register	Address	Description
CCR6	1Dh	Common Control Register 6

3.2 HDLC Controller (section 15)

Register	Address	Description
HCR	B0h	HDLC Control Register
HSR	B1h	HDLC Status Register
HIMR	B2h	HDLC Interrupt Mask Register
RHIR	B3h	Receive HDLC Information Register
RHFR	B4h	Receive HDLC FIFO Register
THIR	B6h	Transmit HDLC Information Register
THFR	B7h	Transmit HDLC FIFO Register
RDC1	B8h	Receive HDLC DS0 Control Register 1
RDC2	B9h	Receive HDLC DS0 Control Register 2
TDC1	BAh	Transmit HDLC DS0 Control Register 1
TDC2	BBh	Transmit HDLC DS0 Control Register 2

3.1.2 Interleaved PCM Bus Operation (section 18)

Register	Address	Description
IBO	B5h	Interleave Bus Operation

3.2 Bit Assignment Changes within Existing Registers

Highlights bit locations in the DS21354/DS21554 which have changed from the DS2154.

Register	Bit #	DS2154 Symbol	DS2154 Description	DS21354/DS21554 Symbol	DS21354/DS21554 Description
CCR3	4	N/A	Not assigned	ESR	Elastic Store Reset
CCR5	6	N/A	Not assigned	RESALGN	Receive Elastic Store Align
CCR5	5	N/A	Not assigned	TESALGN	Transmit Elastic Store Align

4. Changes in Device Pin Out

4.1 Package types

The DS2154 and DS21354/DS21554 are both offered in a 100 pin 14 x 14 x 1.4 mm LQFP. Values listed are for body dimensions.

4.2 Device Pin Differences

4.2.1 JTAG Pins

Pin #	DS21354/DS21554	DS2154	Description
2	JTMS	NC	IEEE 1149.1 Test Mode Select
4	JTCLK	NC	IEEE 1149.1 Test Clock Signal
5	JTRST	NC	IEEE 1149.1 Test Reset
7	JTDI	NC	IEEE 1149.1 Test Data Input
10	JTDO	NC	IEEE 1149.1 Test Data Output

4.2.2 Interleaved PCM Bus Pins

Pin #	DS21354/DS21554	DS2154	Description
36	CI	NC	Carry In
54	CO	NC	Carry Out

4.2.3 Framer Mode Select Pin

Pin #	DS21354/DS21554	DS2154	Description
76	FMS	NC	Framer Mode Select

MORE INFORMATION

DS21354: [QuickView](#) -- [Full \(PDF\) Data Sheet \(624k\)](#) -- [Free Sample](#)

DS2154: [QuickView](#) -- [Full \(PDF\) Data Sheet \(1.1M\)](#) -- [Free Sample](#)

DS21554: [QuickView](#) -- [Full \(PDF\) Data Sheet \(624k\)](#) -- [Free Sample](#)

DS21Q354: [QuickView](#) -- [Full \(PDF\) Data Sheet \(176k\)](#) -- [Free Sample](#)

DS21Q554: [QuickView](#) -- [Full \(PDF\) Data Sheet \(176k\)](#) -- [Free Sample](#)